

# 155Mbps SFP Transceiver with DDMI ATB-PH32-LCDE Series

### **Description:**

The transceiver is a low power, high performance, cost effective module supporting data-rate up to 155Mbps and 20km transmission distance. The low jitter and high sensitivity are extinguished features with TX1550nm/RX1310nm FP laser and PIN/TIA receiver. It incorporates TX\_DIS control, TX-FAULT and RX\_LOS monitor functions. The devices are Class I laser safety compliant.

#### **Application**

- Fast Ethernet
- Switch to switch interface
- SONET/SDH
- Switched backplane applications
- Router/Server interface
- Other optical links



#### **Feature:**

- Compliant with ITU-T G.957
- Compliant with SFP MSA and SFF 8472
- Up to 155Mbps data rate
- 20km transmission with SMF, LC optical interface
- 1310nm/1550nm FP LD and PIN photodetector

## **Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Tst	-40	+85	С
Storage Relative Humidity	RHs	-	95	%
Supply Voltage	Vcc	0	6	V
Voltage on any input/output pin	$V_{IO}$	0	VCC	V

### **Operation Environment:**

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	$V_{CC}$	3.1	3.5	V
Ambient Operating Temperature	$T_{A}$	0	70	С

# **Performance Specification**

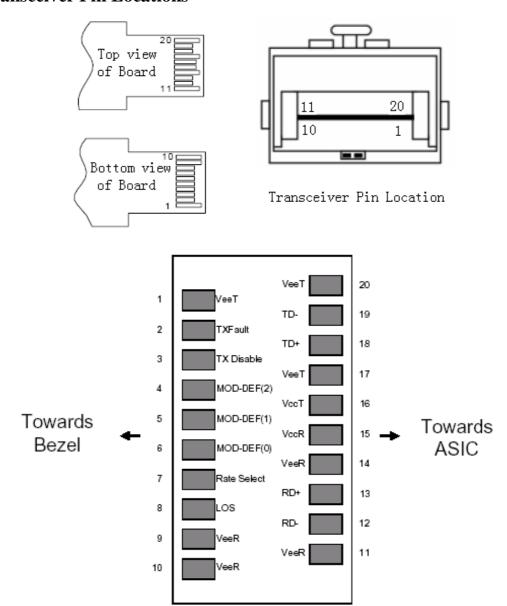
Transmitter Characteristics						
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Supply Voltage	$V_{CC}$	3.1	3.3	3.5	V	
Differential Input Voltage	V <sub>IN</sub>	400	1	1600	mV	
Data Rate	Rate	-	155	-	Mbps	
Optical Output Power	Po	-15	-	-8	dBm	
Extinction Ratio	ER	8.2	-	-	dB	
		1270	1310	1355	nm	ATB-PH22-LCDE
Central Wavelength		1530	1550	1570	nm	ATB-PH32-LCDE
RMS Spectral Width		-	-	3	nm	
Optical Rise/Fall Time	$T_r/T_f$	-	-	2	ns	20~80%
Eye Diagram		Co	omplian	ce with I	ГU-Т G	i.957

Receiver Characteristics						
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Supply Voltage	$V_{CC}$	3.1	3.3	3.5	V	
Differential Output Voltage	V <sub>OUT</sub>	400	1	2000	mV	
Data Rate	Rate	-	155	-	Mbps	
Sensitivity	S	-	-	-34	dBm	1
Optical Input Overload	$P_{OL}$	0	-	-	dBm	
Central Wavelength		1270	1310	1355	nm	ATB-PH32-LCDE
Central Wavelength		1530	1550	1570	11111	ATB-PH22-LCDE
LOS (Loss of Signal)	Optical Decreased	-47	1	-	dBm	
LOS (Loss of Signal)	Optical Increased	1	ı	-36	dBm	
LOS Hysterics	$P_{\mathrm{H}}$	0.5	-	5	dB	

#### Notes:

1. Average received power where the BER =  $10^{-10}$ , measured with a  $2^{23}$ -1 NRZ test pattern..

### **Transceiver Pin Locations**



# **Pin Descriptions**

Pin	Name	Description	Plug Sequence	Note
1	VEET	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	1
3	TX Disable	Transmitter Disable	3	2
4	MOD-DEF2	Module Definition 2	3	3
5	MOD-DEF1	Module Definition 1	3	3
6	MOD-DEF0	Module Definition 0	3	3
7	Rate Select	Not Connected	3	



8	LOS	Loss of Signal	3	4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inverse Received Data Out	3	5
13	RD+	Received Data Out	3	5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power	2	
16	VccT	Transmitter Power	2	
17	VeeT	Transmitter Ground	1	
18	TD+	Transmit Data In	3	6
19	TD-	Inverse Transmit Data In	3	6
20	VeeT	Transmitter Ground	1	

#### Notes:

- 1. TX Fault is an open collector output, which should be pulled up with a  $4.7k\sim10k\Omega$  resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.
- 2. TX Disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a  $4.7k\sim10k\Omega$  resistor. Its states are:

Low (0~0.8V): Transmitter on (>0.8V, <2.0V): Undefined High (2.0~3.5): Transmitter Disabled Open: Transmitter Disabled

3. MOD-DEF 0,1,2 are the module definition pins. They should be pulled up with a  $4.7k\sim10k\Omega$  resistor on the host board. The pull-up voltage shall be VccT or VccR.

MOD-DEF 0 is grounded by the module to indicate that the module is present MOD-DEF 1 is the clock line of two wire serial interface for serial ID MOD-DEF 2 is the data line of two wire serial interface for serial ID

- 4. LOS is an open collector output, which should be pulled up with a  $4.7k\sim10k\Omega$  resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signal. In the low state, the output will be pulled to less than 0.8V.
- 5. These are the differential receiver outputs. They are AC-coupled  $100\Omega$  differential lines which should be terminated with  $100\Omega$  (differential) at the user SERDES.

These are the differential transmitter inputs. They are AC-coupled, differential lines with  $100\Omega$  differential termination inside the module.



## **Digital Diagnostic Monitor Characteristics:**

Parameter	Range	Min	Unit			
Tx Output Power Accuracy	-15~-5	±3.0	dBm			
Rx Input Power Accuracy	-5~-32	±3.0	dBm			
Laser Bias Current Accuracy	5~80	±10	%			
Transceiver Internal Temperature Accuracy	-20~80	±3.0	С			
Transceiver Internal Supply Voltage Accuracy	3.1~3.5	±0.1	V			

# **Serial ID Memory Contents: (A0H)**

Data Address	Length (Byte)	Name of Length	Description and Contents
radiess	(Dyte)	Lengui	Base ID Fields
0	1	Identifier	Type of Serial transceiver (03h=SFP)
1	1	Reserved	Extended identifier of type serial transceiver (04h)
2	1	Connector	Code of optical connector type (07=LC)
3-10	8	Transceiver	OC 3, single mode long reach
11	1	Encoding	8B10B (01h)
12	1	BR,Nominal	Nominal baud rate, unit of 100Mbps
13	2	Reserved	(0000h)
14	1	Length(9um)-km	Link length supported for 9/125 µm fiber, units of km (14h)
15	1	Length(9um)	Link length supported for 9/125um fiber, units of 100m(C8h)
16	1	Length(50um)	Link length supported for 50/125um fiber, units of 10m(00h)
17	1	Length(62.5um)	Link length supported for 62.5/125um fiber, units of 10m(00h)
18	1	Length(Copper)	Link length supported for copper, units of meters(00h)
19	1	Reserved	
20-35	16	Vendor Name	SFP vendor name: Atrie
36	1	Reserved	
37-39	3	Vendor OUI	SFP transceiver vendor OUI ID
40-55	16	Vendor PN	Part Number: "ATB-PH2(3)2-LCDE" (ASCII)
56-59	4	Vendor rev	Revision level for part number
60-62	3	Reserved	
63	1	CCID	Least significant byte of sum of data in address 0-62
			Extended ID Fields
64-65	2	Option	Indicates which optical SFP signals are implemented (001Ah = LOS, TX_FAULT, TX_DISABLE all supported)
66	1	BR, max	Upper bit rate margin, units of %
67	1	BR, min	Lower bit rate margin, units of %
68-83	16	Vendor SN	Serial number (ASCII)



84-91	8	Date code	Atrie's Manufacturing date code
92	1	DDMI Type	Implemented with internal calibration and received power measurement type by Avg. power(68)
93	1	Enhanced options	Alarm/Warning flags monitor are implemented(F0)
94	1	SFF-8472 compliant	SFF-8472 compliant with revision 9.5(02)
95	1	CCEX	Check code for the extended ID Fields (addresses 64 to 94)
		V	Vendor Specific ID fields
96-127	32	Readable	Atrie specific date, read only

# **Serial ID Memory Contents: (A2H)**

Address	# Bytes	Name	2	Description	
00-01	2	Temp High	Alarm	MSB at low address(85 C)	
02-03	2	Temp Low Alarm		MSB at low address(-40 C)	
04-05	2	Temp High V	Varning	MSB at low address(70 C)	
06-07	2	Temp Low V	Varning	MSB at low address(-20 C)	
08-09	2	Voltage High	Alarm	MSB at low address(3.6V)	
10-11	2	Voltage Low	Alarm	MSB at low address(3.0 V)	
12-13	2	Voltage High	Warning	MSB at low address(3.5V)	
14-15	2	Voltage Low	Warning	MSB at low address(3.1V)	
16-17	2	Bias High	Alarm	MSB at low address(80mA)	
18-19	2	Bias Low A	Alarm	MSB at low address(5mA)	
20-21	2	Bias High W	/arning	MSB at low address(50mA)	
22-23	2	Bias Low W	arning	MSB at low address(20mA)	
24-25	2	TX Power Hig	gh Alarm	MSB at low address(-5dBm)	
26-27	2	TX Power Low Alarm		MSB at low address(-18dBm)	
28-29	2	TX Power High	n Warning	MSB at low address(-8dBm)	
30-31	2	TX Power Low	Warning	MSB at low address(-14dBm)	
32-33	2	RX Power Hig	gh Alarm	MSB at low address(-5dBm)	
34-35	2	RX Power Lo	w Alarm	MSB at low address(-34dBm)	
36-37	2	RX Power High	n Warning	MSB at low address(-8dBm)	
38-39	2	RX Power Low	Warning	MSB at low address(-30dBm)	
40-55	16	Reserve	ed	Reserved for future monitored quantities	
Address	# Bytes	Name		Description	
56-59	4	Rx_PWR(4)	Single precision floating point calibration data - Rx optic power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB.		
60-63	4	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB.		
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB.		
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB.		
72-75	4	Rx_PWR(0)	Single precis	ion floating point calibration data, Rx optical of byte 72 is MSB, bit 0 of byte 75 is LSB.	

4			
Atr	íP		SFP Bidi Transceiver with DDMI
			SM, 155Mbps, 20km, TX1550nm/RX1310nm
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB.
78-79	2	Tx_I(Offset)	Fixed decimal (signed two's complement) calibration data , laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte81 is LSB.
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB.
84-85	2	T(Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB.
86-87	2	T(Offset)	Fixed decimal (signed two's complement) calibration data internal module temperature. Bit 7 of byte 86 is MSB, bit 0
80-87	2	T(Offset)	of byte 87 is LSB.
88-89	2	V(Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB.
90-91	2	V(Offset)	Fixed decimal (signed two's complement) calibration data internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB.
02.05	4	D 1	•
92-95	4	Reserved	Reserved
Byte	4 Bit	Name	Reserved <b>Description</b>
		Name	
		Name	<b>Description</b> analog values. Calibrated 16 bit data
Byte	Bit	Name Converted	<b>Description</b> analog values. Calibrated 16 bit data
<b>Byte</b> 96	Bit All	Name Converted Temperature MSB	<b>Description</b> analog values. Calibrated 16 bit data
<b>Byte</b> 96 97	Bit All All	Name Converted Temperature MSB Temperature LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.
96 97 98	All All All	Name Converted Temperature MSB Temperature LSB Vcc MSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.
96 97 98 99	All All All All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB	Description  analog values. Calibrated 16 bit data  Internally measured module temperature.  Internally measured supply voltage in transceiver.
96 97 98 99	All All All All All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB	Description  analog values. Calibrated 16 bit data  Internally measured module temperature.  Internally measured supply voltage in transceiver.
96 97 98 99 100 101	All All All All All All All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB	Description  analog values. Calibrated 16 bit data  Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.
96 97 98 99 100 101 102	All All All All All All All All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB	Description  analog values. Calibrated 16 bit data  Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.
96 97 98 99 100 101 102 103	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB	Description  analog values. Calibrated 16 bit data  Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.
96 97 98 99 100 101 102 103 104	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB TX Power LSB	Description  analog values. Calibrated 16 bit data  Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.
96 97 98 99 100 101 102 103 104 105	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power LSB RX Power LSB	Description  analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.
96 97 98 99 100 101 102 103 104 105 106	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power LSB RX Power LSB RX Power LSB RX Power LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.  Reserved for 1st future definition of digitized analog input
96 97 98 99 100 101 102 103 104 105 106 107	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power LSB RX Power LSB RX Power LSB Reserved MSB Reserved LSB Reserved LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.  Reserved for 1st future definition of digitized analog input Reserved for 1st future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input
96 97 98 99 100 101 102 103 104 105 106 107 108 109	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power LSB RX Power LSB Reserved MSB Reserved LSB Reserved LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.  Reserved for 1st future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Optional Status/Control Bits
96 97 98 99 100 101 102 103 104 105 106 107 108	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power LSB RX Power LSB RX Power LSB Reserved MSB Reserved LSB Reserved LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.  Reserved for 1st future definition of digitized analog input Reserved for 1st future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Optional Status/Control Bits Digital state of the TX Disable Input Pin. Not supported.
96 97 98 99 100 101 102 103 104 105 106 107 108 109	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power LSB RX Power LSB Reserved MSB Reserved LSB Reserved LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.  Reserved for 1st future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Optional Status/Control Bits
96 97 98 99 100 101 102 103 104 105 106 107 108 109	All	Name Converted Temperature MSB Temperature LSB Vcc MSB Vcc LSB TX Bias MSB TX Bias LSB TX Power MSB TX Power MSB RX Power LSB RX Power LSB Reserved MSB Reserved LSB	Description analog values. Calibrated 16 bit data Internally measured module temperature.  Internally measured supply voltage in transceiver.  Internally measured TX Bias Current.  Measured TX output power.  Measured RX input power.  Reserved for 1st future definition of digitized analog input Reserved for 1st future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Reserved for 2nd future definition of digitized analog input Optional Status/Control Bits  Digital state of the TX Disable Input Pin. Not supported. Read/write bit that allows software disable of laser. Not

2

110

110

Soft RX Rate

Select

TX Fault

Read/write bit that allows software RX rate select.

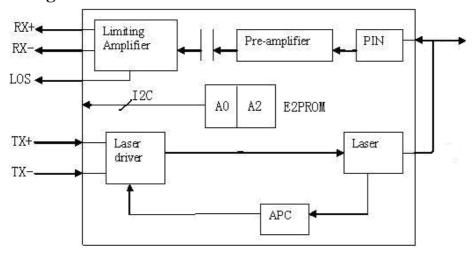
Not supported.

Digital state of the TX Fault Output Pin.



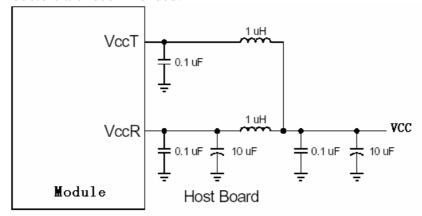
110	1	LOS	Digital state of the LOS Output Pin.
110	0	Data Ready	Indicates transceiver has achieved power up and data is ready
111	7-0	Reserved	Reserved.
Byte	Bit	Name	Description
			ptional Alarm and Warning Flag Bits
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
112	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
112	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
112	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
112	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
112	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
112	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
113	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
113	0~5	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
116	6	Temp Low Warning	Set when internal temperature is below low warning level.
116	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
116	4	_	Set when internal supply voltage is below low warning level.
116	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
116	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
116	1	TX Power High Warning	Set when TX output power exceeds high warning level.
116	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
117	6	RX Power Low Warning	Set when Received Power is below low warning level.
117	0~5	Reserved Warning	
118	All	Reserved	
119	All	Reserved	
120-127	8	Vendor Specific	00h.
128-255	128		

#### **Block Diagram**

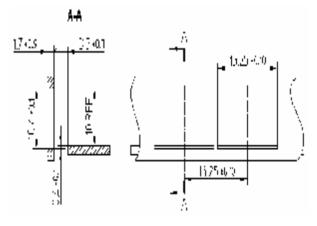


## **Power Supply**

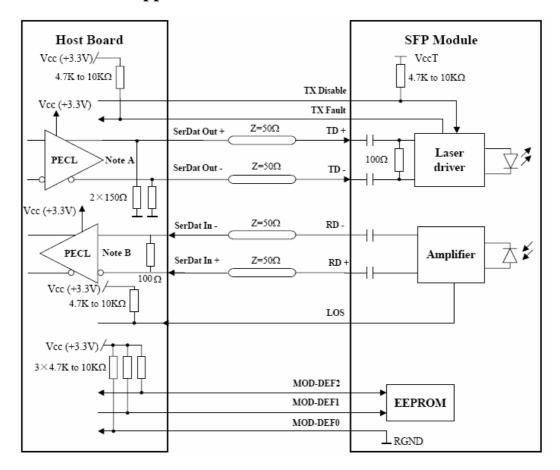
The Transceiver includes internal circuit components to filter power supply noise. Under some conditions of EMI and power supply noise, external power supply filtering may be necessary. If receiver sensitivity is found to be degraded by power supply noise, the filter network illustrated in the following figure may be used to improve performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.



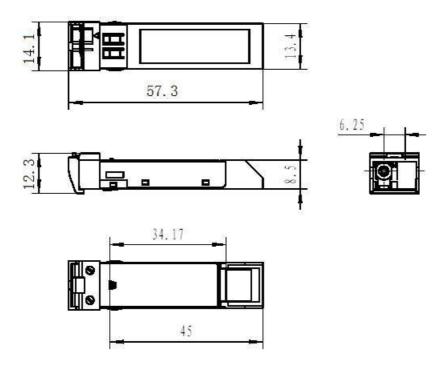
# **Recommended Front Panel Layout Opening for LC**

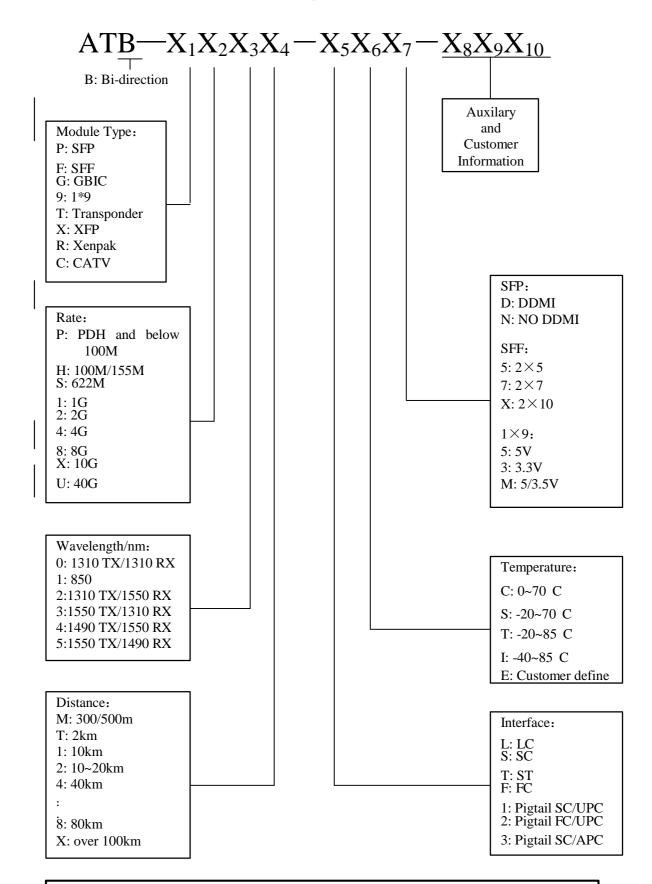


## **Recommended Application Circuits**



# **Outline Specification**





Note: Atrie Technology Inc. reserves all the rights to make changes in product design, features, capabilities, function, or specifications at any time without notice.